Exploiting on-chip Parallelism with Hybrid MPI/OpenMP Programming

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Today most systems in high-performance computing (HPC) feature a hierarchical hardware design: Shared memory nodes with several multi-core CPUs are connected via a network infrastructure. In this presentation we discuss the possibility of employing a hierarchical programming model on such hardware. The model under consideration is hybrid MPI/OpenMP parallelization. We describe potentials and challenges of pure MPI and pure OpenMP and explore the use of hybrid MPI/OpenMP in various flavors. Several case studies are presented where the hybrid approach is of advantage. Pitfalls, limitations and challenges will also be discussed.